In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-28. (Canceled)

29. (Currently Amended) A solder bump for interconnection of flip chip devices comprising:

~~a substrate, active semiconductor devices having been created in or over said substrate;~~

a semiconductor surface;

at least one contact pad ~~created~~ over said ~~substrate~~ semiconductor surface;

a ~~patterned layer of~~ passivation ~~created~~ layer over said ~~substrate~~ semiconductor surface, said ~~patterned layer of~~ passivation layer exposing said at least one contact pad;

an ~~patterned layer of~~ Under-Bump-Metallurgy (UBM) ~~created~~ layer over said layer of passivation~~, including~~ and said at least one contact pad,~~a surface area~~ lateral dimension of the ~~patterned layer of~~ UBM layer being limited to~~a size no larger than a size of~~ be within a ~~surface area~~ lateral dimension of the at least one contact pad; and

at least one ~~layer of reflown~~ solder compound overlying the ~~patterned layer of~~ UBM layer, wherein the solder compound comprises an approximately flat top surface and convex sidewalls before connecting to other components.

30. (Currently Amended) The solder bump of claim 29, said ~~layer of~~ Under Bump Metallurgy layer comprising a layer of chromium followed by a layer of copper followed by a layer of gold.

31. (Currently Amended) The solder bump of claim 29, said ~~layer of~~ Under Bump Metallurgy layer comprising a plurality of sub-layers of different metallic composition.

32. (Currently Amended) The solder bump of claim 29, said ~~patterned layer of~~ passivation layer comprising a plurality of passivation layers.

33. (Original) The solder bump of claim 32, wherein at least one of said plurality of passivation layers is PE Si_3N_4, SiO_2 a photosensitive polyimide, phosphorous doped silicon dioxide or titanium nitride.

34. (Original) The solder bump of claim 29, said at least one contact pad on said semiconductor surface being electrically connected with a semiconductor device with at least one conductive line of interconnect or with at least one conductive contact point.

35. (Cancelled)

36. (Currently Amended) The solder bump of claim 29, ~~with~~ further comprising a seed layer having been deposited over said patterned layer of passivation.

37. (New) A solder bump for interconnection of flip chip devices comprising:

a semiconductor surface;

at least one contact pad over said semiconductor surface;

a passivation layer over said-semiconductor surface, said passivation layer exposing said at least one contact pad;

an Under-Bump-Metallurgy (UBM) layer over said passivation layer and said at least one contact pad, lateral dimension of the UBM layer being limited to a size approximately the same as lateral dimension of the at least one contact pad; and

at least one solder compound overlying the UBM layer.

38. (New) A solder bump for interconnection of flip chip devices comprising:

a semiconductor surface;

at least one contact pad over said semiconductor surface;

a passivation layer over said-semiconductor surface, said passivation layer exposing said at least one contact pad;

an Under-Bump-Metallurgy (UBM) layer over said passivation layer and said at least one contact pad; and

at least one solder compound overlying the UBM layer, wherein the solder compound comprises an approximately flat top surface and convex sidewalls before connecting to other components.